Please amend the present application as follows:

Specification

The following is a copy of Applicant's specification that identifies language being added with underlining ("___") and language being deleted with strikethrough ("~~—~~"), as is applicable:

Page 3, lines 25 through 26.

FIG. 9 ~~and~~ is a phase diagram illustrating a non-limiting example of third-order harmonics cancellation by the low harmonics frequency division system of FIG. 7.

Page 5, lines 3 through 15.

Baseband subsystem 110 also includes analog-to-digital converter (ADC) 124 and digital-to-analog converters (DACs) 126, 130 and 132. ADC 124, DAC 126, DAC 130 and DAC 132 communicate with microprocessor 112, memory 114, analog circuitry 116 and DSP 118 via data bus 122. DAC 126 converts digital communication information within baseband subsystem 110 into an analog signal for transmission to RF subsystem 134 via connection 142. In accordance with an aspect of the invention, DAC 130 provides a reference voltage power level signal to power control element 152 via connection 120 and DAC 132 provides an amplitude modulated (AM) signal to power control element 152 via connection 160. Alternatively, circuitry (not shown) could be placed in power control element 152 to derive the AM signal based on the output of DAC 126 received via connection 142. Connection 142, while shown as two directed arrows,

includes the information that is to be transmitted by RF subsystem 134 after conversion from the digital domain to the analog domain.

Page 6, lines 3 through 7.

A portion of the amplified transmit signal energy on connection 164 is supplied via connection 166 to power control element 152. Power control element 152 ~~152,~~ forms a closed power control feedback loop and supplies an AM component of the transmit signal via connection 162 to power amplifier 158 and also supplies a power control feedback signal via connection 154 to upconverter 150.

Page 8, lines 4 through 8.

The states "1" and "0" in Table 1 are commonly referred to as "high" and "low" states, respectively, and are typically represented by distinguishable voltage levels such as, for example, "positive" and "negative" voltages, or "higher" and "lower" voltages. The relationships between the inputs and outputs of each of the storage elements 202 and 204 may also be described by ~~to~~ the following logic equation:

Pages 12, line 26 through page 13, line 8.

FIG. 9 ~~and~~ is a phase diagrams 900 illustrating a non-limiting example of third-order harmonics cancellation by low harmonics frequency division system 700. Phase diagram 900 includes a "real" axis 902 and an "imaginary" axis 904. Third harmonic components 906 and 908 are contained in signals 706 and 708, respectively (FIG. 7). Components 906 and 908 have the same magnitude but are 180° out of phase. Therefore,

by combining signals 706 and 708, third harmonic components 906 and 908, respectively, can effectively cancel each other. Although, for illustration purposes, harmonic components 906 and 908 are shown to have phase angles of 90° and 270°, respectively, the phase angles may in fact have any respective values that are substantially 180° apart.

Page 13, line 19 through page 14, line 9.

The bases of transistors 1002 and 1020 are coupled together and to a connection 1012 that contains an incoming signal ϕ. In addition, the bases of transistors 1004 and 1018 are coupled together and to a connection 1010 containing an incoming signal /ϕ (where /ϕ is the inverse of ϕ). The collectors of transistors 1002 and 1018 are coupled together, and to an output connection 1014 containing an output signal D-CLK. The collectors of transistors 1004 and 1020 are also coupled together, and to an output connection 1016 containing an output signal Q-CLK (where Q-CLK is the inverse D-CLK).

CLK and /CLK represent a differential pair of input clock signals, ϕ and /ϕ represent a differential pair of phase control signals, and Q-CLK and D-CLK represent a differential pair of output clock signals. When ϕ is high and /ϕ is low, transistors 1002 and 1020 are active and transistors 1004 and 1018 are inactive. As a result, CLK is passed through transistors ~~1006~~ 1005 and 1002 to connection 1014 to form output clock signal D-CLK, and /CLK is passed through transistors ~~1008~~ 1007 and 1020 to connection 1016 to form output Q-CLK. Conversely, when ϕ is low and /ϕ is high, transistors 1004 and 1018 are active and transistors 1002 and 1020 are inactive. As a result, CLK is passed through transistors ~~1006~~ 1005 and 1004 to connection 1016 to form output signal

Q-CLK, and input /CLK is passed through transistors 1007 and 1018 to connection 1014 to form output D-CLK.

Page 15, lines 7 through 25.

With continued reference to FIG. 11, FIG. 12 is a simplified timing diagram 1200 illustrating the operation of storage element 1100 as part of a "divide by three" frequency divider, such as, for example, frequency divider 500 (FIG. 5). For illustration purposes, timing diagram 1200 does not show gradual transitions between states and does not show all possible inputs and outputs. The timing diagram 1200 shows the following signals: CLK 1202, /CLK 1204, ϕ 1206, D-CLK 1208, Q-CLK 1210, D 1212, and Q 1214. These signals (1202, 1204, 1206, 1208, 1210, ~~and~~ 1212, and 1214) may correspond, for example, to the signals carried by connections 1006, 1008, 1012, 1014, 1016, 1108, and 1122, respectively.

CLK 1202, /CLK 1204, ϕ 1206, and D 1212 are input signals; D-CLK 1208 and Q-CLK 1210 are internal storage element signals ~~are~~ that are based on input signals 1202, 1204, and 1206; and Q 1214 is an output signal that is based on the input D 1212 and the internal signals D-CLK 1208 and Q-CLK 1210. The state of D-CLK 1208 is substantially equivalent to the state of CLK 1202 when ϕ 1206 is high (for example, between t_0 and t_3), and is substantially equivalent to the state of /CLK 1204 when ϕ 1206 is low (for example, between t_3 and t_6). Q-CLK 1210 is effectively the inverse of D-CLK. Therefore, the state of D-CLK 1208 is substantially equivalent to the state of /CLK 1204 when ϕ 1206 is high (for example, between t_0 and t_3), and is substantially equivalent to the state of CLK 1202 when ϕ 1206 is low (for example, between t_3 and t_6).